A HIGH PERFORMANCE SWITCHED-LNA IC FOR CDMA HANDSET RECEIVER APPLICATIONS

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ABSTRACT

This paper reports on a low voltage, low noise, high linearity amplifier with on-chip bypass switch to provide extended dynamic range. The amplifier is designed for the wide dynamic range requirements of cellular band CDMA handsets. In high gain mode, the amplifier achieves 16.5dB gain, 1.5dB noise figure and 0dBm input IP3 with just 10mA of current from a 2.7V supply. In bypass mode, the input IP3 increases to +27dBm with <5dB insertion loss and <100uA of DC current. This patented M/A-COM topology switched- LNA is fabricated on M/A-COM's 0.5um low noise MESFET process and packaged in a low cost 8 lead MSOP plastic package.

INTRODUCTION

Low voltage, high performance LNAs play a crucial role in portable wireless receiver design. High gain and very low noise figures have been reported using many different circuit topologies and process technologies (1-3). The trade-off is always made however, between noise figure and IP3 in order to achieve a wide dynamic range receiver.

CDMA systems require receivers with very wide dynamic range. When the mobile station is at the edge of a cell, very low noise figure is necessary to detect the low power desired signal from the surrounding noise which will include other users on the same channel. On the other hand, when the handset is very close to the base-station, the data must not be corrupted by non-linearities in the receiver due to the high signal levels. Both scenarios translate to a receiver requirement of very low noise figure and a very high input IP3. However, it is not necessary to achieve both requirements simultaneously. For instance, at low input power levels, low noise figure is essential while a reasonable level of input IP3 is necessary to prevent de-sensitization of the receiver due to an interfering signal. On the other hand, at high input power levels, high noise figure is of little consequence, but very high IP3 is essential. For this reason, most CDMA receiver topologies incorporate some form of gain control in the receive chain which changes the system from a low noise, high gain state to a low gain, high IP3 state.

The LNA at the front end of the receiver plays a significant role in setting the noise figure and input IP3 of the complete chain. High gain and low noise figure are essential for a low noise receiver while low gain and high IP3 optimize the input IP3 of the chain -- the conflicting requirements are obvious. Therefore, incorporating gain control which switches the LNA from a high gain, low noise state to a lossy, high IP3 state, allows the performance of the complete receiver to be effectively adapted to the power level of the input signal.

Some previously described methods of gain control in the LNA include variation of the bias current in the amplifier transistors (3) or

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use of a variable voltage attenuator(VVA) between stages of the LNA (4). Both of these methods effectively decrease the gain but have the disadvantage of also degrading the IP3 of the LNA. A possible discrete solution using single-pole double-throw switches at the input and output of the amplifier is shown in fig. 1. This topology allows switching from a high gain state to a low gain, high IP3 state. However, the noise figure in the high gain state will be significantly degraded by the loss of the input switch.

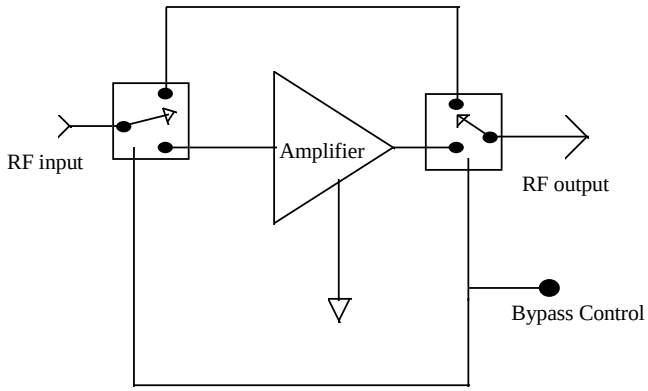

Fig.1: Switched LNA using 2 single-pole double-throw switches

The patented circuit topology shown in fig 2 achieves the low gain and high IP3 of a bypass state without sacrificing any noise figure performance in the high gain state. The operation of this new circuit is such that in high gain mode, the off-chip bipolar transistor is 'on' and the amplifier is biased 'on' via the self bias resistor. The bypass switch is 'off' and thus has a minimal effect on the amplifier performance allowing very low noise figure and high gain to be achieved, while the input IP3 is set by the bias current in the amplifier FETs. By adjusting the control voltage, the bipolar transistor turns 'off', thus turning off the amplifier while the bypass switch is simultaneously turned 'on'. The signal is now attenuated by the loss in the bypass switch and the input IP3 is essentially the IP3 of the switch. This topology also has the added advantage of almost zero (leakage only) dc current in the low gain mode.

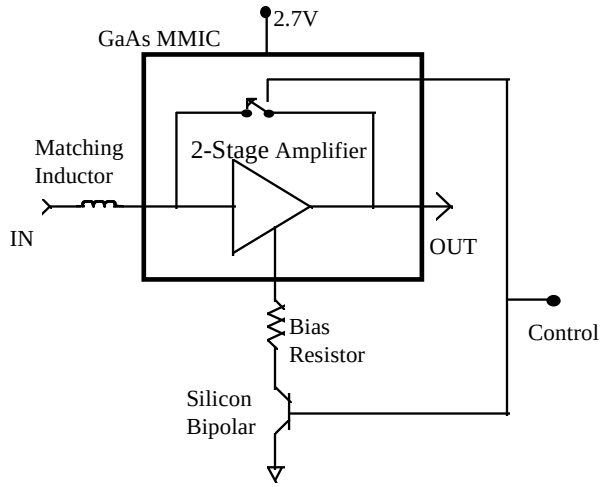

Fig 2: M/A-COM Switched-LNA Block Diagram

CIRCUIT DESIGN

The circuit schematic is shown in fig. 3. The amplifier is a 2 stage common source cascade with the sources bypassed off chip using capacitors Cb1 and Cb2, and the drain currents set using the self-bias resistor Rb. The circuit is designed with 5mA per stage but by decreasing Rb, the current can be increased to obtain higher input IP3 in the high gain mode. An off-chip inductor Lin, matches the input for optimum noise performance in the band of interest.

The bypass switch consists of 2 series FETs with gates grounded and drain and source voltages controlled by the control voltage Vctl. Blocking capacitors at the input and output of the switch insure no dc current flow and thus that the drain and source voltages are equal.

When the amplifier is 'on', the switch FETs have the effect of capacitive feedback from output to input which can cause instability. Careful attention was therefore paid to achieving unconditional stability at all frequencies. Meanwhile, the parallel bypass switch has minimal effect on the gain and noise figure performance of the amplifier.

When the control voltage is switched from 2.7V to 0V, the bypass FETs have 0V

gate-to-source and are thus 'on'. Simultaneously, the off-chip bipolar transistor is turned 'off', causing the amplifier source voltages to be pulled up to ~2.7V. The gate-source voltage is now -2.7V and the amplifier FETs are 'off' with the total leakage current being set by the bipolar transistor. The loss in the switch mode is essentially the loss of 2 FETs in series, with some additional loss due to the input and output matching elements.

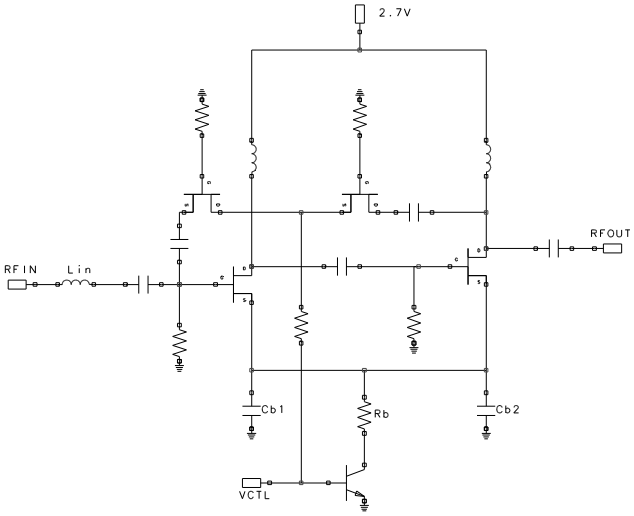

Fig.3: Switched LNA Schematic

PERFORMANCE

The circuit was fabricated on M/A-COM's 0.5um low noise MESFET process. This process has been extensively characterized with small and large signal statistical FET models. The circuit, including plastic package model, was simulated on HP-EESOF Libra Series IV; extensive use was made of the statistical design tools to insure a high yielding product.

Figures 4, 5 and 6 show measured data for the plastic packaged amplifier. The plots show the gain, noise figure, and input IP3 in the 800-1000MHz band for both modes of operation. In high gain mode, the amplifier has more than 16dB gain with <1.5dB noise figure in the 869-894MHz cellular receive band. An input IP3 of 0dBm is achieved at the bias level of 2.7V and 10mA. In bypass mode the insertion loss is 4.8dB and the input IP3 increases to +27dBm.

Fig. 7 shows a cascade analysis of a typical receiver and demonstrates the effect of the switched LNA on the performance of the complete receive chain. As shown in the diagram, switching from high gain mode to bypass mode in the LNA, has the effect of increasing the input IP3 of the receiver from -10dBm to +12dBm, an increase of 22dB. Because the mode switching occurs only when the input power levels are high, the increase in noise figure from 2.1dB to 15dB will not effect the integrity of the data.

CONCLUSION

The design of a low voltage, high performance LNA for the 900MHz cellular band has been described. 16dB gain, 1.5dB noise figure and 0dBm input IP3 was achieved across the 869-894MHz band with just 10mA from a 2.7V DC supply. Through the use of a zero-current bypass mode, the device can be switched to achieve +27dBm input IP3 with 4.8dB insertion loss thereby extending the dynamic range of the receiver. The performance makes the device attractive for cellular handset receivers, especially in CDMA applications where very wide dynamic range is required.

Acknowledgment:

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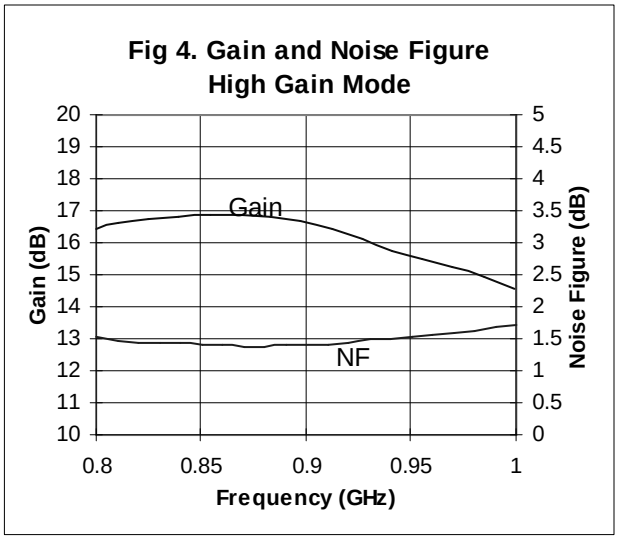

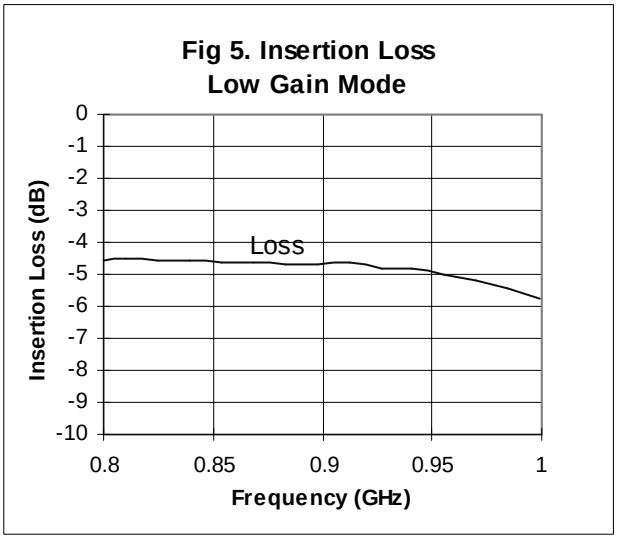

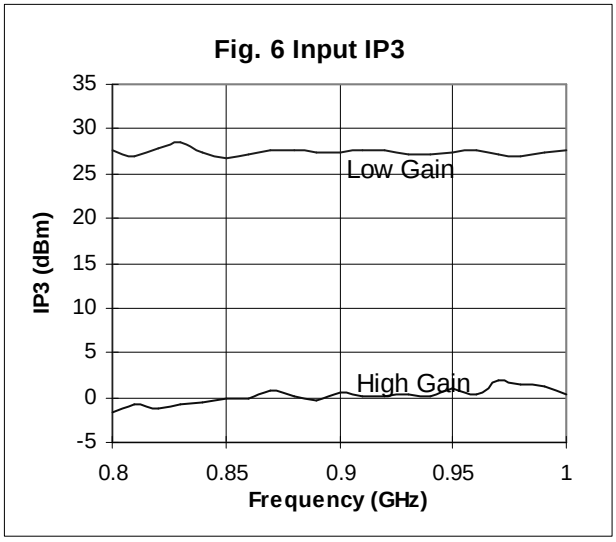

		LNA	Filter	RFA	Mixer	IFA	Cascade
	Gain (dB)	16.5	-3	8	-8	11.5	25
High Gain	NF (dB)	1.5	3	3.5	8	5	2.1
	IIP3 (dBm)	0	∞	11	16	8.5	-9.8
	Gain (dB)	-5	-3	8	-8	11.5	3.5
Low Gain	NF (dB)	5	3	3.5	8	5	15
	IIP3 (dBm)	27	∞	11	16	8.5	12

Fig. 7: Chain analysis of receiver in high and low gain modes